

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Shunpei YAMAZAKI et al.) ATTN: New Applications
Based On: JP 2002-276379)
Filed: September 20, 2002)
For: MANUFACTURING METHOD)
OF SEMICONDUCTOR DEVICE)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, Applicant submits herewith a Form PTO-1449 listing references known to Applicant and requests that these references be made of record in the above identified application. Copies of the references listed are submitted herewith in accordance with 37 C.F.R. 1.98(a).

U.S. Patent No. 6,475,912 is in the family of Japanese Patent Laid-Open No. 2000-58650.

U.S. Patent Publication 2001/0015618 is in the family of Japanese Patent Laid-Open No. 2001-236025.

U.S. Patent Publication 2001/0030322 is in the family of Japanese Patent Laid-Open No. 2001-313397.

U.S. Patent No. 6,413,845 is in the family of Japanese Patent Laid-Open No. 2000-357671.

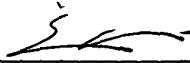
The Examiner's attention is also directed to related U.S. Patent Application Serial No. 10/245,701.

The Commissioner is hereby authorized to charge fees under 37 C.F.R. §§1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be

required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

A duplicate copy of this sheet is attached.

Respectfully submitted,



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				Filing Date	
				First Named Inventor	
				Group Art Unit	
				Examiner Name	
Sheet	2	of	2	Attorney Docket Number	
0756-7196					

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
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Examiner Initials ¹	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		Stanley Wolf "4.5.6.3 Contact-Hole and Via Filling with Selective Electroless Metal Deposition," Silicon Processing for the VLSI Era, Vol. 2, Process Integration, pp. 256-257	
		M. Hatano et al., "A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance," IEDM 97, pp. 523-526	
		U.S. Patent Application Serial No. 10/245,701 entitled Semiconductor Device and Method of Manufacturing the Same filed 09/18/2002	

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Sheet	1	of	2	Attorney Docket Number	
				0756-7196	

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		M.A. Baldo et al., "Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices," Nature, Vol. 395, September 10, 1998, pp. 151-154	

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